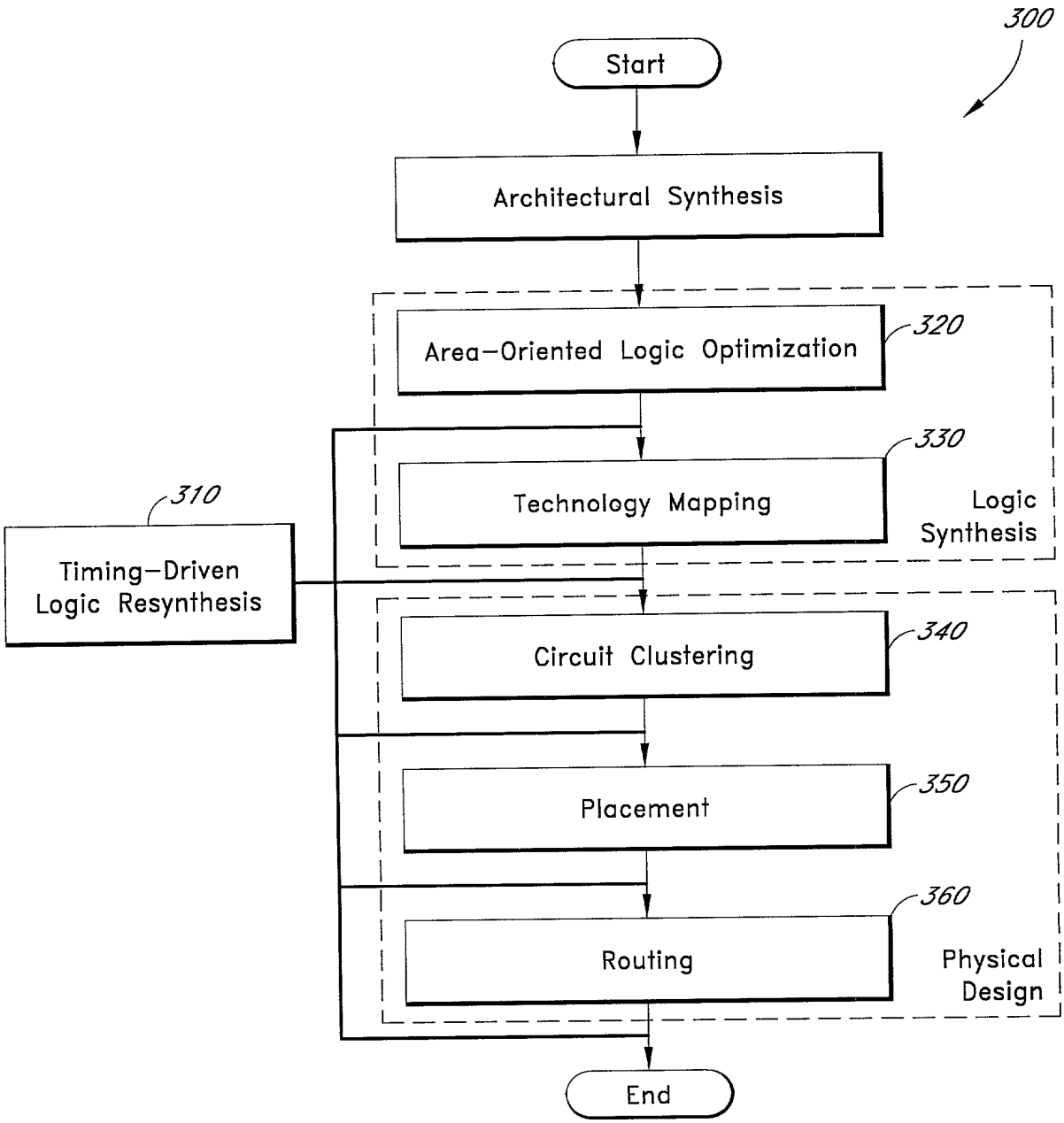

300
Start
Architectural Synthesis
Area-Oriented Logic Optimization
320
330
Technology Mapping
Logic Synthesis
310
Timing-Driven Logic Resynthesis
Circuit Clustering
340
Placement
350
360
Routing
Physical Design
End

FIG. 1

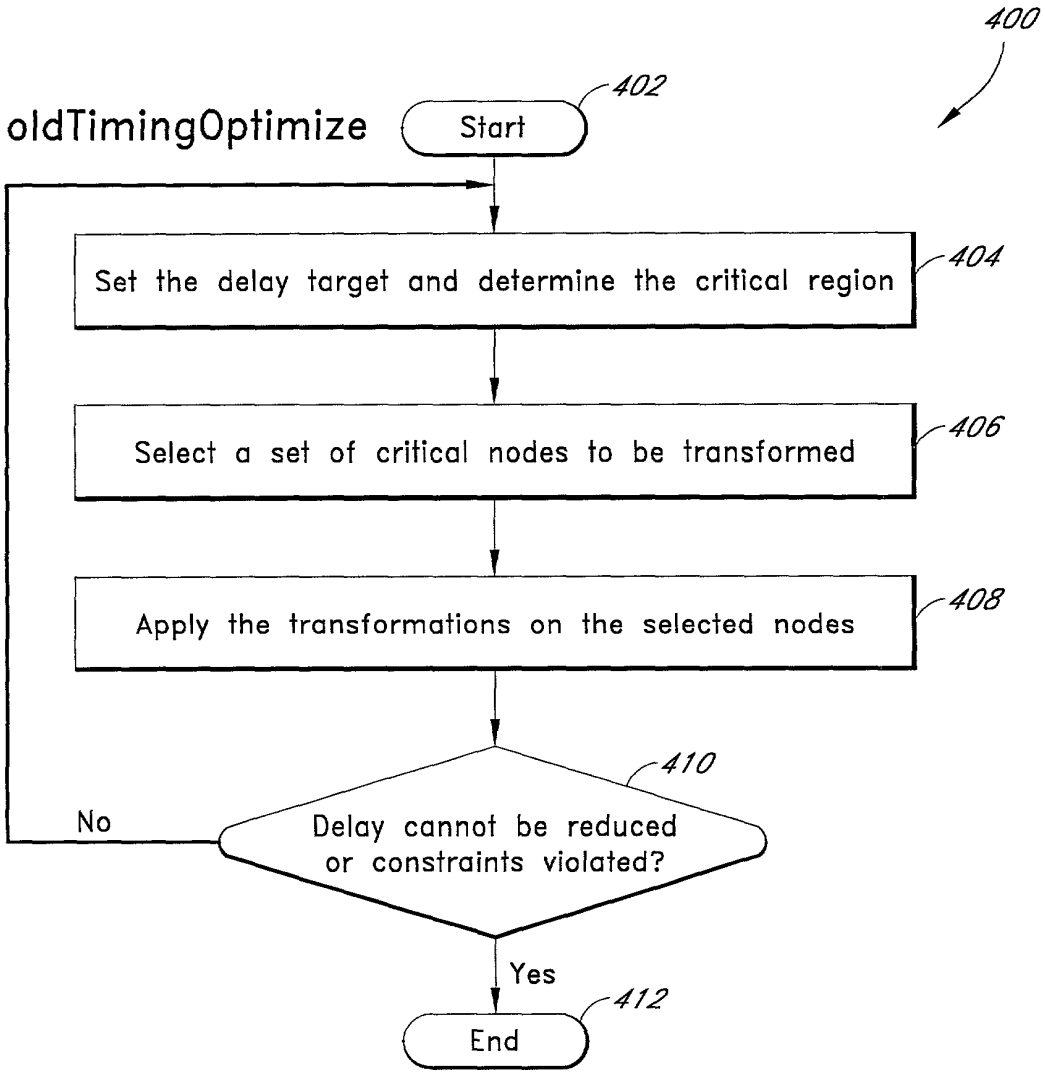

400
oldTimingOptimize
Start
402
Set the delay target and determine the critical region
404
Select a set of critical nodes to be transformed
406
Apply the transformations on the selected nodes
408
Delay cannot be reduced or constraints violated?
410
No
Yes
End
412

FIG. 2

Local Transformation

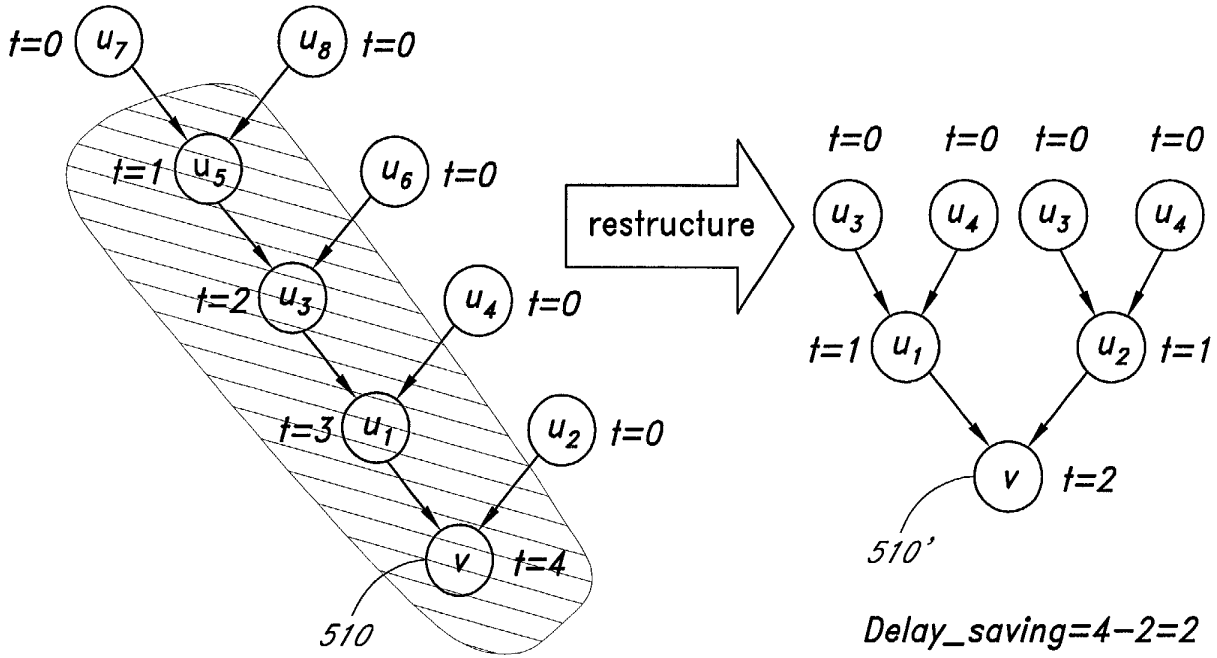


FIG. 3

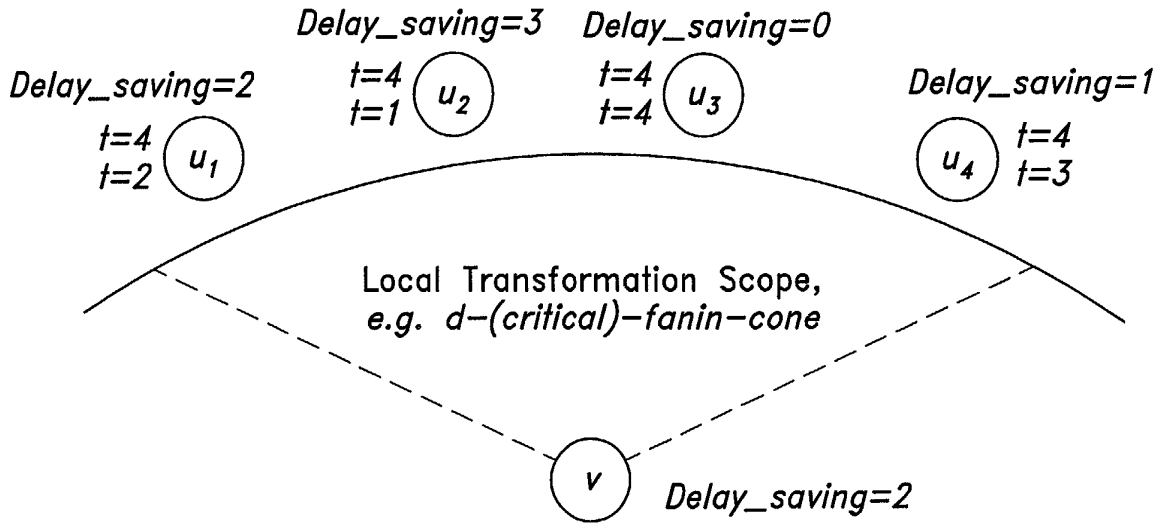

Delay_saving=3
Delay_saving=0
Delay_saving=2
t=4
t=1
u2
t=4
t=4
u3
t=4
t=2
u1
Delay_saving=1
u4
t=4
t=3
Local Transformation Scope,
e.g. d-(critical)-fanin-cone
v
Delay_saving=2

FIG. 4

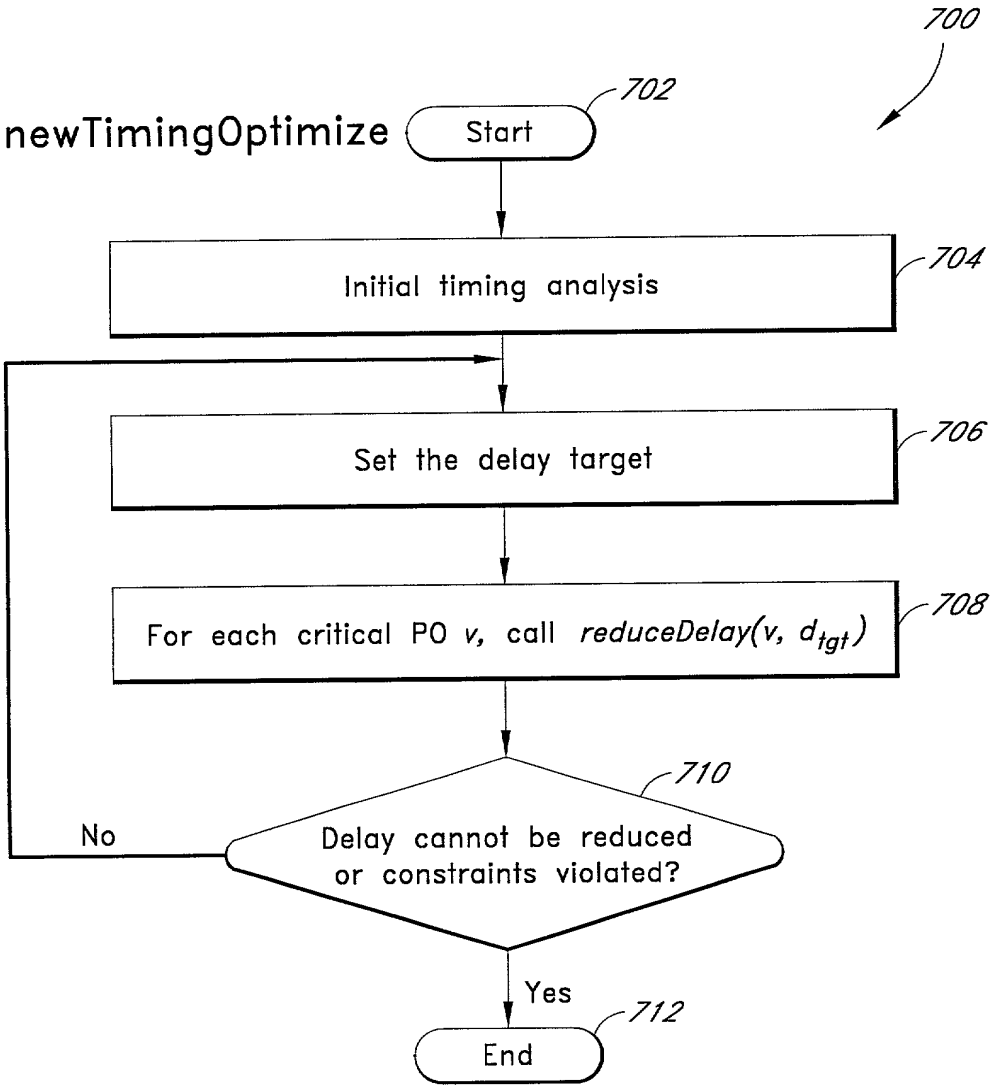

700
newTimingOptimize
Start
702
Initial timing analysis
704
Set the delay target
706
For each critical PO v, call reduceDelay(v, d_{tgt})
708
Delay cannot be reduced or constraints violated?
710
No
Yes
End
712

FIG. 5

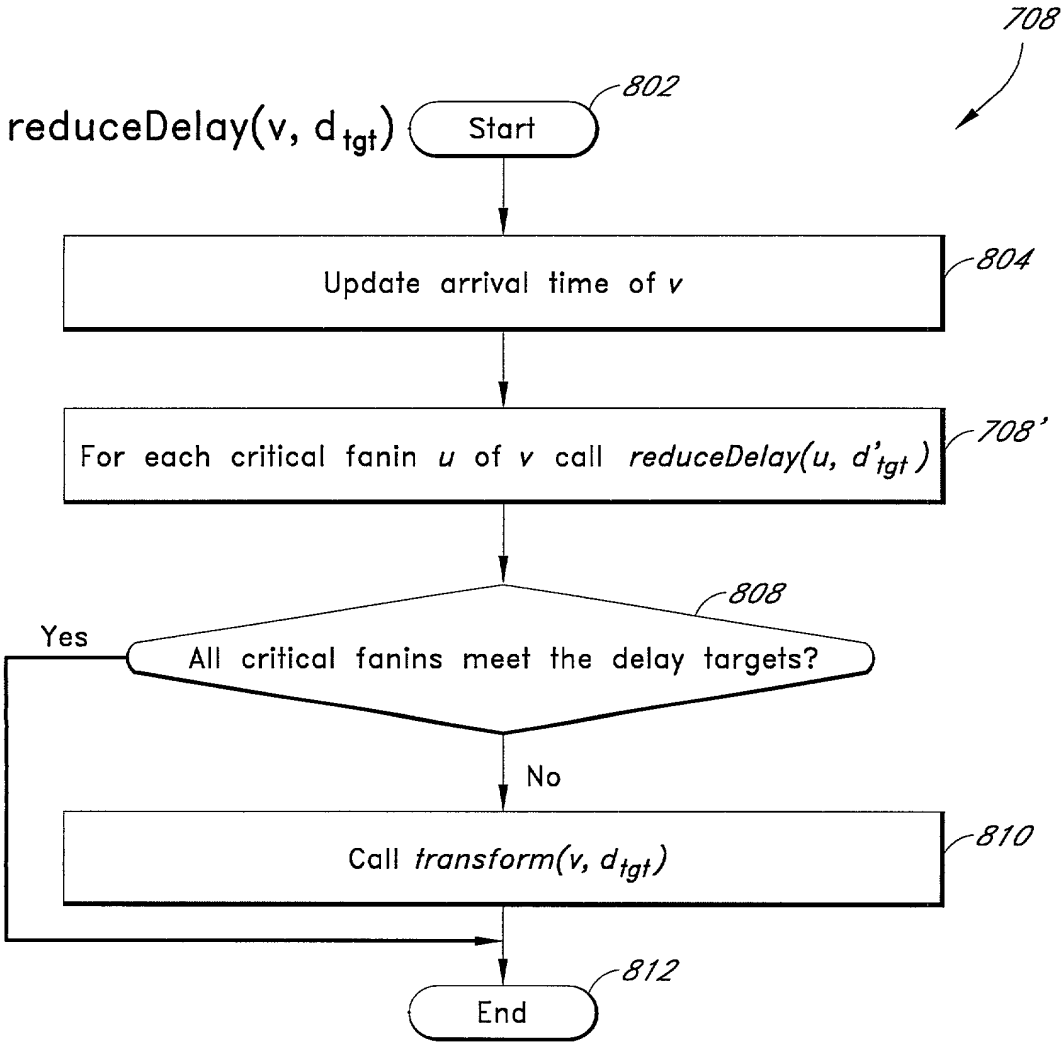

708
reduceDelay(v, d tgt)
802
Start
Update arrival time of v
804
For each critical fanin u of v call reduceDelay(u, d'tgt)
708'
808
Yes
All critical fanins meet the delay targets?
No
Call transform(v, dtgt)
810
812
End

FIG. 6

Example of Recursive Delay Reduction

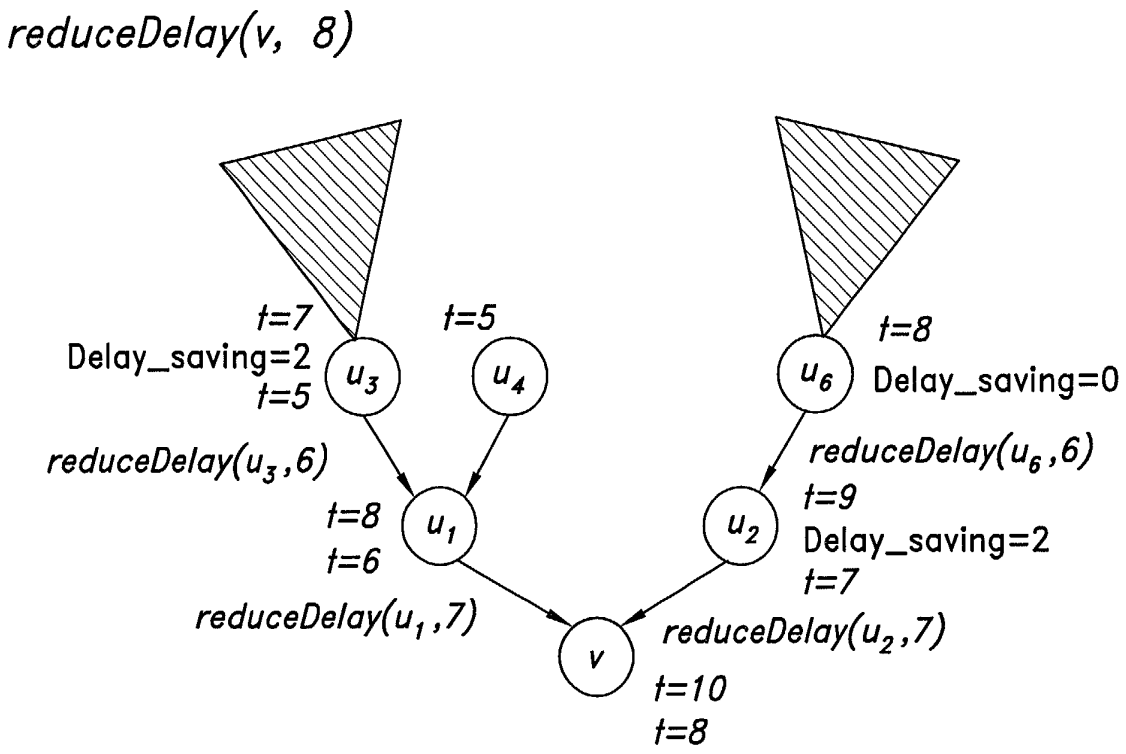
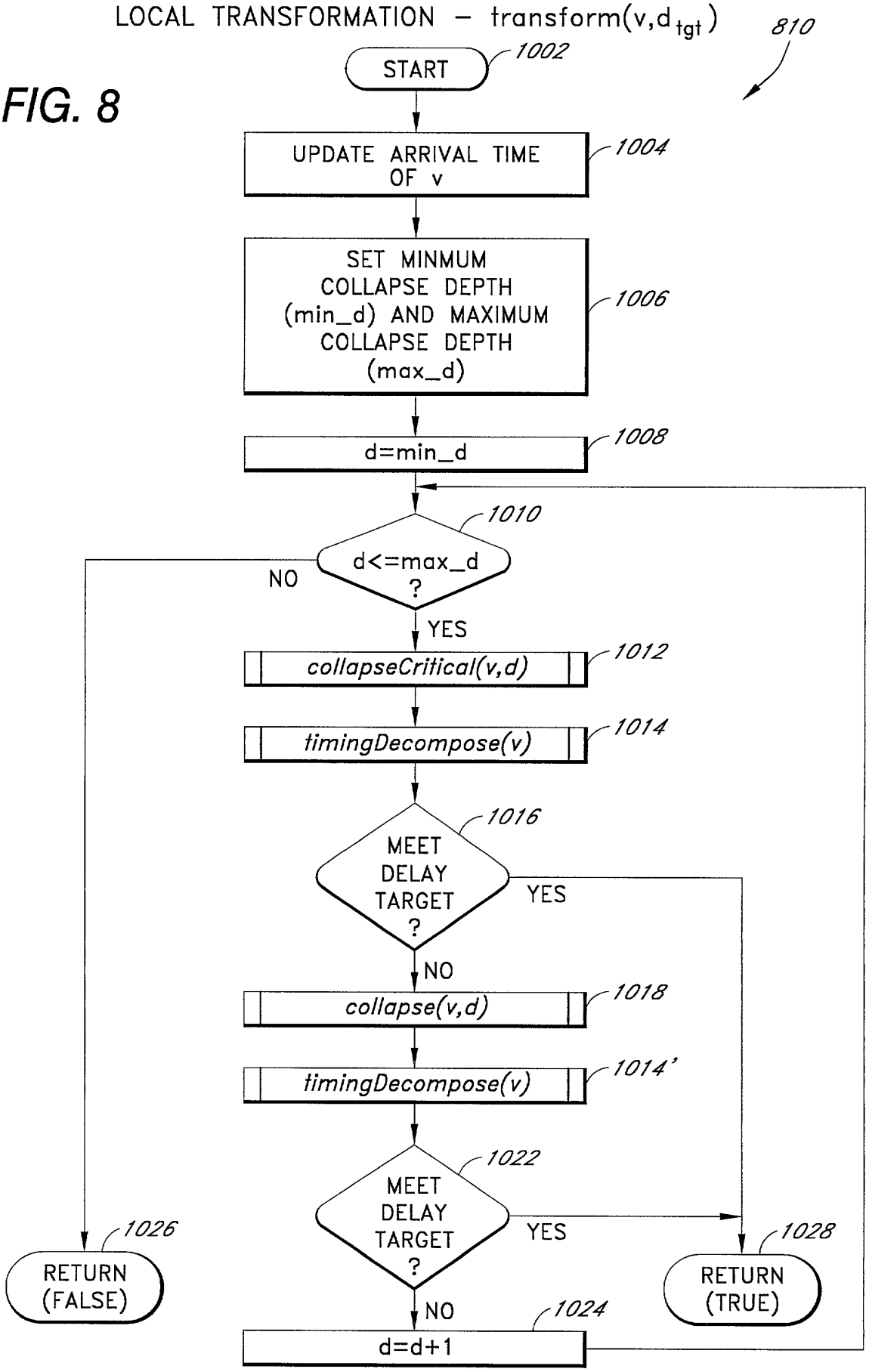


FIG. 7

FIG. 8


LOCAL TRANSFORMATION – transform(v,d tgt)
810
START
1002
UPDATE ARRIVAL TIME OF v
1004
SET MINMUM COLLAPSE DEPTH (min_d) AND MAXIMUM COLLAPSE DEPTH (max_d)
1006
d=min_d
1008
1010
d<=max_d ?
NO
YES
collapseCritical(v,d)
1012
timingDecompose(v)
1014
1016
MEET DELAY TARGET ?
YES
NO
collapse(v,d)
1018
timingDecompose(v)
1014'
1022
MEET DELAY TARGET ?
YES
NO
1024
d=d+1
1026
RETURN (FALSE)
1028
RETURN (TRUE)

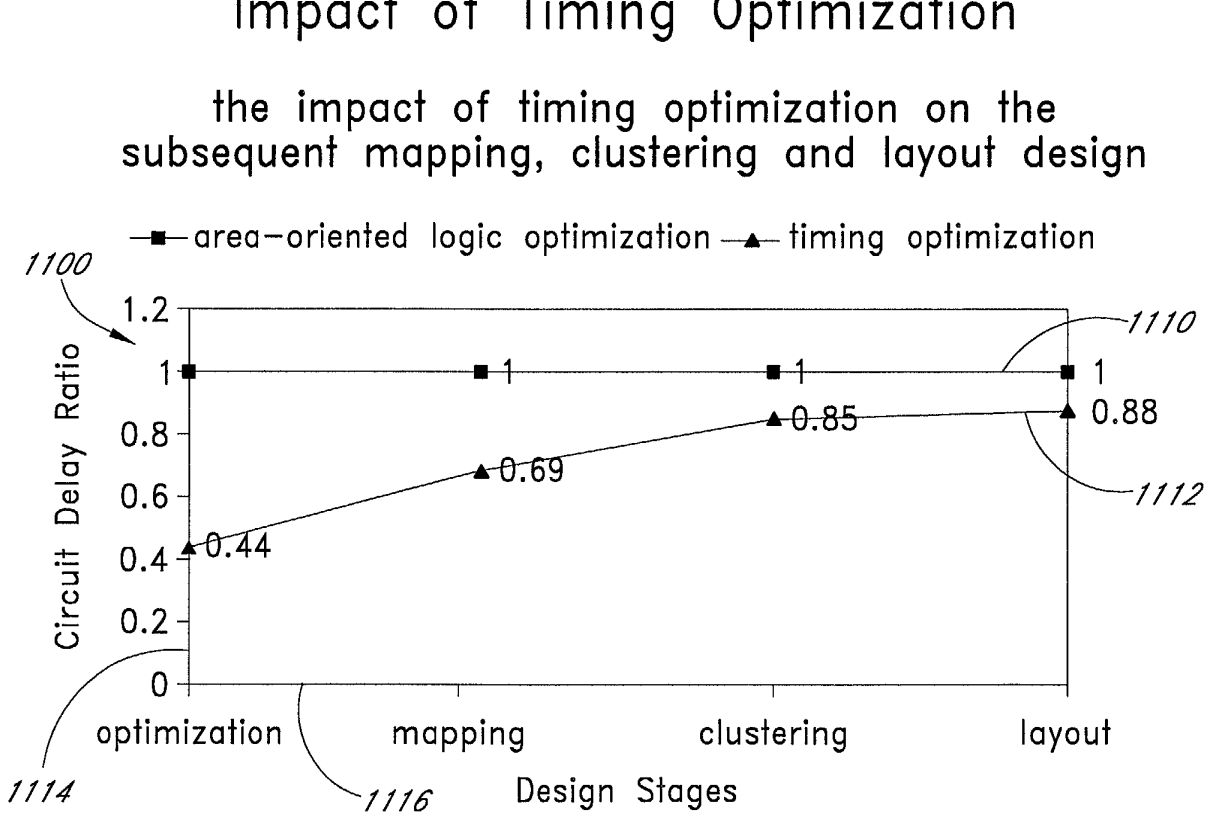

Impact of Timing Optimization
the impact of timing optimization on the subsequent mapping, clustering and layout design
area-oriented logic optimization
timing optimization
1100
1110
1112
1114
1116
Circuit Delay Ratio
1.2
1
0.8
0.6
0.4
0.2
0
1
1
1
0.44
0.69
0.85
0.88
optimization
mapping
clustering
layout
Design Stages

FIG. 9

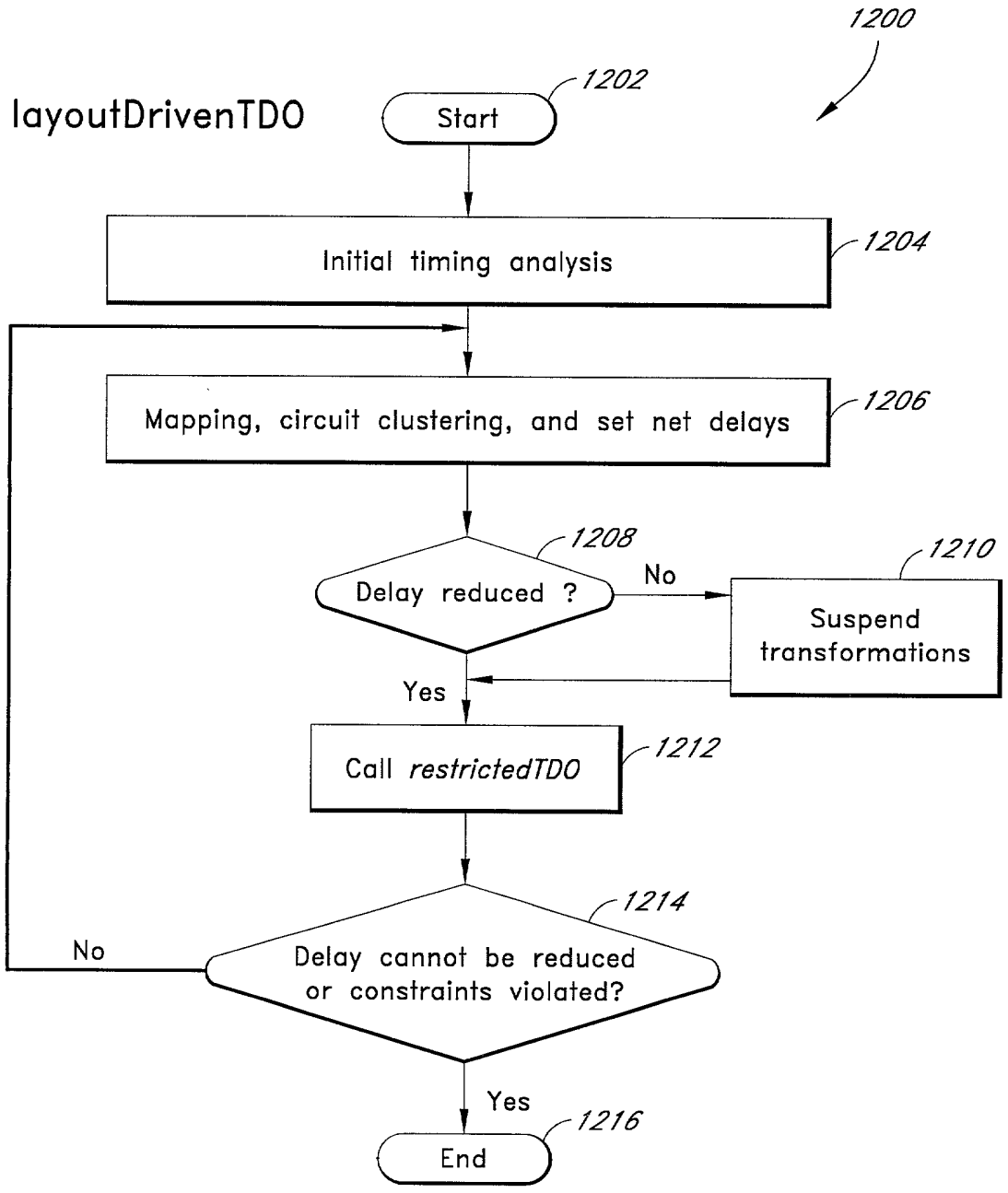

1200
layoutDrivenTDO
Start
1202
Initial timing analysis
1204
Mapping, circuit clustering, and set net delays
1206
Delay reduced ?
1208
No
Suspend transformations
1210
Yes
Call restrictedTDO
1212
Delay cannot be reduced or constraints violated?
1214
No
Yes
End
1216

FIG. 10